Electronic Version
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Claims

[c1] A method of manufacturing a structure, comprising the steps of:
providing a structure having an insulator layer with at least one interconnect;
forming a sub lithographic template mask over the insulator layer; and
selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect.

[c2] The method of claim 1, wherein the sub lithographic features are substantially vertical columns in the insulator layer.

[c3] The method of claim 2, wherein the sub lithographic features further include a plurality of holes formed in a capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer.

[c4] The method of claim 1, wherein the etching step is an anisotropic etching forming a plurality of the sub lithographic features defined as nano columns.

[c5] The method of claim 4, wherein the etching step includes an isotropic etching to meld at least adjacent nano columns together and provide an undercut below the at least one interconnect.

[c6] The method of claim 1, wherein:
the sub lithographic features are substantially vertical columns in the insulator layer;
the sub lithographic features further include a plurality of holes having a diameter less than a diameter of the at least one interconnect and substantially equal to the substantially vertical columns in the insulator layer and a top portion of the holes are tapered.

[c7] The method of claim 1, further comprising the step of depositing a capping layer prior to the forming step and pinching off a top portion of the capping layer to form pinched off structures having a sub lithographic diameter.

[c8] The method of claim 7, further comprising the step of depositing an insulating layer on the portion to form the pinched off structures.

[c9] The method of claim 8, wherein the depositing step forms insulator material on the sidewalls of the at least one interconnect, which was etched away during the etching step.

[c10] 10. The method of claim 1, wherein the sub lithographic template mask is a block copolymer nanotemplate formed on a diffusion layer, the diffusion layer acting as a mask having features transferred from the block copolymer nanotemplate.

[c11] The method of claim 10, wherein the block copolymer nanotemplate has features smaller than spacings between adjacent interconnects.

[c12] The method of claim 10, wherein the block copolymer nanotemplate is a material which self assemblies itself into substantially uniformly shaped and spaced holes or features.

[c13] The method of claim 10, wherein the features of the block copolymer nanotemplate 150 are in a range from below 5 nm to 100 nm.

[c14] The method of claim 1, wherein the block copolymer nanotemplate is formed one of (i) partially over a block-out resist over the insulation layer and (ii) below the

blockout resist, the blockout resist includes features that are larger than a spacing between adjacent interconnects.

[c15] The method of claim 14, further comprising the step of removing the block copolymer nanotemplate and blockout resist after the formation of the sub lithographic features in the insulation layer.

[c16] The method of claim 15, further comprising the step of providing a capping layer over the insulation layer.

[c17] The method of claim 1, wherein the sub lithographic template mask is a metal deposition layer which is treated to cause agglomeration.

[c18] The method of claim 17, wherein the metal deposition layer includes a material of one of Au, Ag, In, Sn and Ga.

[c19] The method of claim 17, wherein the agglomeration is formed by annealing and the agglomeration creates sub lithographic features in the range of 1 nm to 50 nm.

[c20] The method of claim 19, wherein the annealing causes nano islands which are used as a mask in an etching step.

[c21] The method of claim 17, wherein the metal deposition layer is deposited over a capping layer.

[c22] The method of claim 21, wherein the capping layer is formed from material from one of SiN, SiC and SiCOH

[c23] The method of claim 21, further comprising the steps of :

etching the capping layer though the sub lithographic features formed in the metal deposition layer to form pores corresponding to the features in the metal deposition layer;

removing the metal deposition layer; and

etching the insulation layer using the capping layer as a mask to form the sub lithographic features.

[c24] The method of claim 23, wherein the sub lithographic features are substantially vertical pores.

[c25] The method of claim 24, further comprising melding together adjacent vertical pores between the at least one interconnect.

[c26] The method of claim 23, wherein the sub lithographic features are backfilled with a second material than that of the insulation layer.

[c27] The method of claim 23, further comprising the step of providing a sealing cap over the sub lithographic features.

[c28] The method of claim 1, wherein the sub lithographic features are backfilled with a second material than that of the insulation layer.

[c29] The method of claim 27, wherein the sealing cap is selected from a material of SiN or SiC having a thickness in the range from 5 nm to 50 nm.

[c30] The method of claim 27, further comprising the step of depositing an insulator material on the sealing cap layer with a different characteristic.

[c31] The method of claim 1, wherein the sub lithographic template mask is formed from a random hole pattern in resist using e-beam, x-ray or EUV lithography.

[c32] The method of claim 1, wherein the sub lithographic template mask is a random hole pattern in a 2-phase polymer mask using a porogen.

[c33] The method of claim 1, further comprising the step of forming a diblock patterning mask beneath the sub lithographic template mask.

[c34] The method of claim 1, further comprising providing a supra lithographic mask either over or underneath the sub lithographic template mask.

[c35] The method of claim 34, wherein the supra lithographic mask prevents formation of gaps over at least one area whose dimensions are larger than a minimum interconnect spacing.

[c36] A method of manufacturing a structure, comprising the steps of:
providing a structure having an insulator layer with a plurality of interconnects;
forming an insulating diffusion barrier layer on the insulator layer;
forming a blocking structure on the insulating diffusion barrier layer;
forming a sub lithographic template mask on the insulating diffusion barrier layer having sub lithographic features;
selectively etching the insulating diffusion barrier layer and the insulator layer through the sub lithographic template mask to form sub lithographic features in the insulator layer.

[c37] The method of claim 36, wherein the blocking structure is formed one of under and over the sub lithographic template mask.

[c38] The method of claim 36, wherein the sub lithographic features include a plurality of holes having a diameter

less than a diameter of each of the plurality of interconnects and smaller than vertical columns formed in the insulator layer.

[c39] The method of claim 36, wherein the etching step includes an anisotropic etching and an isotropic etching to dissolve partitions between the sub lithographic features and provide an undercut below at least one of the plurality of interconnects.

[c40] The method of claim 36, wherein:
the sub lithographic features are substantially vertical columns in the insulator layer;
the sub lithographic features further include a plurality of holes in the insulating diffusion barrier layer having a diameter or cross section is approximately equal to a diameter or cross section of the substantially vertical columns in the insulator layer.

[c41] The method of claim 40, further comprising the step of pinching off the top portion of the holes with a capping layer.

[c42] The method of claim 36, wherein:
the sub lithographic template mask includes a block copolymer nanotemplate with features ranging from below 5 nm to 100 nm; and

the blocking structure is a diblock mask.

[c43] The method of claim 36, wherein the sub lithographic template mask is a metal deposition layer which is treated to cause agglomeration, the agglomeration creating nano meter scale islands which are used as a mask in the etching step.

[c44] The method of claim 36, wherein the sub lithographic features are backfilled with a second material than that of the insulation layer.

[c45] The method of claim 36, further comprising the steps of :

depositing a sealing cap over the sub lithographic features in the insulator layer to form pinch offs; and depositing an insulator material on the sealing cap layer.

[c46] The method of claim 36, wherein the sub lithographic template mask is formed from one of (i) a random hole pattern in resist using e-beam, x-ray or EUV lithography and (ii) a random hole pattern in a 2-phase polymer mask using porogen.

[c47] The method of claim 36, wherein the etching step removes insulator material from sidewalls of the plurality of interconnects and the insulator material is later redeposited thereon.

[c48] The method of claim 36, further comprising depositing insulation material over the sub lithographic features to form pinched off sections and to provide insulation material on the sidewalls of some of the plurality of interconnects.

[c49] A semiconductor structure, comprising:
an insulator layer having at least one interconnect feature; and
at least one gap formed in the insulator layer spanning more than a minimum spacing of the interconnects.

[c50] The structure of claim 49, further comprising a plurality of sub lithographic features formed on a top portion of the insulator layer and communicating with the at least one gap, the plurality of sub lithographic features having a diameter less than any of the at least one gap.

[c51] The structure of claim 50, wherein the sub lithographic features are pinched off portions communicating with the at least one gap.

[c52] The structure of claim 51, further comprising a sealing layer formed over the insulator layer for pinching off the each of at least one gap.

[c53] The structure of claim 52, wherein the pinched off por-

tions are formed in a diffusion barrier layer deposited on the insulator layer.

[c54] The structure of claim 51, wherein the at least one gap includes insulator material on a side wall adjacent to the at least one interconnect feature.

[c55] he structure of claim 54, wherein the at least one gap and the plurality of sub lithographic features each have a cross section less than that of the at least one interconnect.

[c56] The structure of claim 49, wherein the gaps are absent in a scribe lane.

[c57] The structure of claim 49, wherein the gaps are absent near vias.